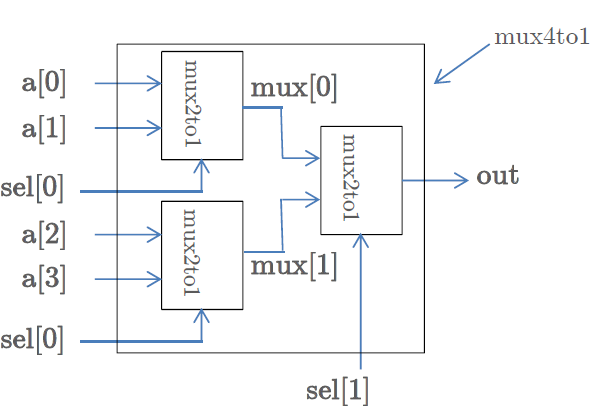
****

**module mux41 (I, Sel, Out);**

**input [3:0] I;**

**input [1:0] Sel;**

**output Out;**

**wire [1:0] m;**

**mux21 m1 (I[0], I[1], Sel[0], m[0]);**

**mux21 m2 (I[2], I[3], Sel[0], m[1]);**

**mux21 m3 (m[0], m[1], Sel[1], Out);**

**endmodule**

**--------------------------------------------------**

**module mux41 (I, Sel, Out);**

**input [3:0] I;**

**input [1:0] Sel;**

**output Out;**

**reg Out;**

**always @ (\*)**

**case (Sel)**

**2'd0: Out=I[0];**

**2'd1: Out=I[1];**

**2'd2: Out=I[2];**

**2'd3: Out=I[3];**

**default: Out=0;**

**endcase**

**endmodule**

**--------------------------------------------------**

**module mux41 (I, Sel, Out);**

**input [3:0] I;**

**input [1:0] Sel;**

**output Out;**

**reg Out;**

**always @ (I, Sel)**

**case (Sel)**

**2'b00: Out=I[0];**

**2'b01: Out=I[1];**

**2'b10: Out=I[2];**

**2'b11: Out=I[3];**

**default: Out=0;**

**endcase**

**endmodule**

**--------------------------------------------------**

**module mux41 (I, Sel, Out);**

**input [3:0] I;**

**input [1:0] Sel;**

**output Out;**

**reg Out;**

**always @ (I, Sel)**

**if (Sel==2'b00)**

**Out=I[0];**

**else if (Sel==2'b01)**

**Out=I[1];**

**else if (Sel==2'b10)**

**Out=I[2];**

**else if (Sel==2'b11)**

**Out=I[3];**

**else**

**Out=0;**

**endcase**

**endmodule**

**--------------------------------------------------**

**module TestModule; //test bench to test mux41 (4-to-1 MUX)**

**// Inputs**

**reg [3:0] In;**

**reg [1:0] S;**

**// Outputs**

**wire Out;**

**// Instantiate the Unit/Design Under Test (U/DUT)**

**mux41 dut (.Sel(S), .I(In), .Out(O));**

**initial begin**

**// Initialize Inputs**

**In = 4'b1010;**

**S = 2'b11;**

**#100**

**In = 4'b1011;**

**S = 2'b10;**

**#150**

**In = 4'b1101;**

**S = 2'b10;**

**end**

**endmodule**